GaAs Wafer Dicing Technologies

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Abstract

Gallium arsenide (GaAs) has a higher electron mobility than silicon (Si) and, as a direct bandgap semiconductor, is widely used as a substrate material for high-frequency devices as well as for light-emitting devices operating in the red to near-infrared wavelength range. However, due to its high brittleness and the resulting difficulty in processing, GaAs presents significant challenges in wafer singulation. In addition to conventional mechanical dicing using blades (abrasives), laser-based dicing techniques have therefore been increasingly applied. This paper describes the various dicing methods used for GaAs substrates and discusses their respective characteristics.

1. Introduction

Blade-based dicing using abrasives is widely applied to GaAs substrates as a low-cost processing method. However, in order to suppress chipping during processing, the cutting speed must be kept low. In particular, thinned GaAs substrates are highly brittle and prone to cracking, making high-quality mechanical processing difficult.

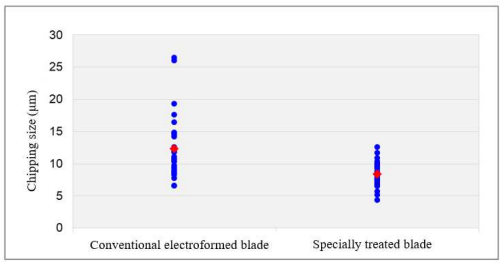
In recent years, driven by the widespread adoption of mobile devices such as smartphones, demand has increased for thin and compact GaAs-based chips, including high electron mobility transistors (HEMTs) and vertical cavity surface emitting lasers (VCSELs). As a result, there is a growing need to achieve both high processing quality and high productivity. To meet these requirements, laser dicing has been introduced as an alternative approach, with two primary processing modes being employed: ablation and stealth dicing.

2. Dicing Technologies and Their Characteristics

2.1 Blade Dicing

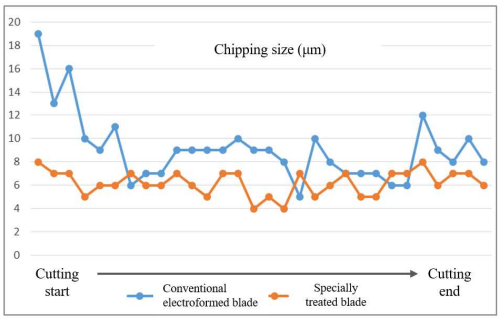
Because blade dicing is a cutting method in which an abrasive (blade) mounted on a high-speed rotating spindle physically contacts the wafer, chipping inevitably occurs due to this mechanical interaction between the blade and the wafer. To prevent chipping from exceeding the street width on the wafer, appropriate blade selection and optimization of the cutting recipe are required. In general, it is well known that chipping becomes more severe as the wafer becomes thinner and the target chip size becomes smaller. Therefore, minimizing the cutting resistance during processing is critical to reducing the chipping size.

To address this issue, a conventional electroformed blade and a blade subjected to a special surface treatment designed to reduce cutting resistance were prepared, and the resulting chipping sizes generated during dicing were compared, as shown in Fig. 1. The results demonstrate that the use of the specially treated blade reduced the chipping size by approximately 32% on average.



Wafer: GaAs φ150 mm, Thickness: 100 µm
Cut size: 0.3 mm x 0.3 mm
Cut speed: 10 mm/s

Fig. 1 Surface chipping size



Wafer: GaAs φ150 mm, Thickness: 100 µm
Cut size: 0.3 mm x 0.3 mm
Cut speed: 10 mm/s

Fig. 2 Backside chipping size trend

Next, Fig. 2 shows the time evolution of the chipping size from the start to the end of the cutting process. When the specially treated blade was used, the chipping size remained stable throughout the entire process. In contrast, for the blade without special treatment, the chipping size at the beginning of the cut was more than twice as large and required a certain amount of time to stabilize. Such large chipping at the initial stage of cutting can be partially mitigated by performing a pre-cut using silicon or GaAs dummy wafers; however, complete suppression is difficult to achieve. Moreover, prolonged pre-cutting degrades productivity and increases cost.

Processing with the specially treated blade not only addresses these issues related to productivity and cost but also enables narrowing of the street width through chipping size reduction, thereby contributing to an increase in the number of chips obtained per wafer.

2.2 Ablation Laser Dicing

Ablation is a processing method in which laser irradiation is applied to the surface of the material, causing instantaneous sublimation and vaporization. Compared with blade dicing, this approach is effective in suppressing chipping. However, a key challenge is the reduction in chip flexural strength due to thermal damage induced by the laser energy.

Conventionally, as shown in Process 1 in Fig. 3, wet etching has been employed to remove the thermally damaged layer and thereby improve the flexural strength of the chips. However, because process complexity and the cost and environmental burden associated with chemical usage have become significant concerns, there has been a shift toward the process shown as Process 2 in Fig. 3. In this approach, a water-soluble protective film is applied to the wafer surface and subsequently removed after dicing using only DI water cleaning.

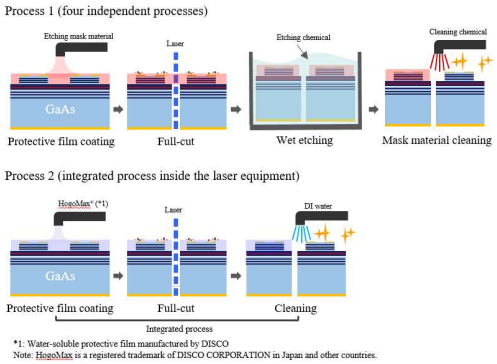
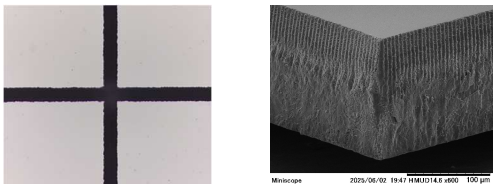


Fig. 3 Process flow comparison

Since this process does not involve wet etching, optimization of the processing sequence, including laser energy, scanning speed, and other recipe parameters, to minimize thermal damage during processing is essential. By applying an optimized recipe, chip flexural strength comparable to that achieved with the conventional process was obtained. Images of the chip top surface and cross section after processing are shown in Fig. 4.

To further improve productivity, a high-output laser oscillator and a specialized optical system designed to suppress heat accumulation were developed. This enabled processing at a net cutting speed approximately seven times higher than that of the conventional process while maintaining product quality. Images of the chip top surface and cross section after processing are shown in Fig. 5.

Because this process eliminates the need for wet etching and thereby reduces environmental impact, it is expected to become widely adopted as a mass-production process.

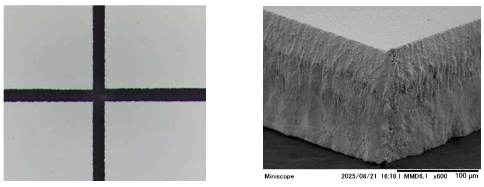


Top side (microscope mag. x100) Cross section (SEM)

Wafer: GaAs φ150 mm, Thickness: 150 μm
Cut size: 0.1 mm x 0.1 mm
Net cut speed (*1): 16 mm/s

Fig. 4 Photographs after processing with Process 2

*1: Converted speed based on the assumption that, when a single cut line is processed using multiple cut sequences, it is completely cut through in one scan.
Scan count X at cut speed a
Scan count Y at cut speed b
Net speed = 1 / [(1/a) × X + (1/b) × Y]



Top side (microscope mag. x100) Cross section (SEM)

Wafer: GaAs φ150 mm, Thickness: 150 μm
Cut size: 0.1 mm x 0.1 mm
Net cut speed: 117 mm/s

Fig. 5 Photographs after processing using the new laser oscillator and optical system

2.3 Stealth Dicing™

Stealth Dicing is a dicing technique in which a laser is focused inside the wafer to form a modified layer, and the chips are subsequently separated by initiating fracture from this modified layer. In recent years, the number of applications to VCSELs and HEMTs fabricated on GaAs substrates has been increasing. Stealth dicing is a dry process that does not require water, and its high processing speed enables a reduction in running costs. In addition, because separation is achieved by internal cracking, kerf loss is negligible, allowing the street width to be significantly reduced and the number of chips obtained per wafer to be increased. Figure 6 shows top-view and cross-sectional images of GaAs chips processed by stealth dicing. These images demonstrate that high-speed and high-quality processing can be achieved.

Another application example is edge-emitting diodes. In stealth dicing, after internal modification, the wafer is cleaved along the crystal cleavage planes, allowing these planes to be used as the light extraction surfaces of edge-emitting diodes. The chip fabrication method for edge-emitting diodes is shown in Fig. 7. To prevent direct laser irradiation of the light extraction surface, a HASEN cut, where the laser is selectively turned

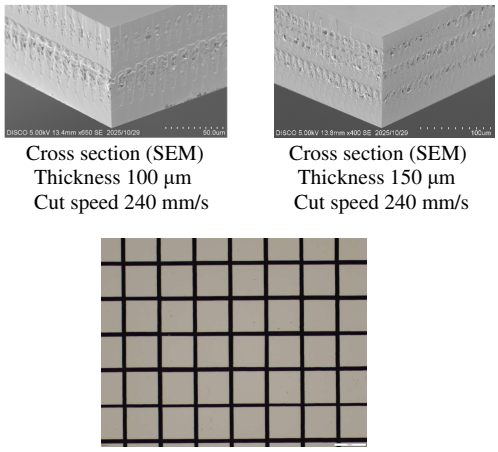


Fig. 6 Cross-sectional SEM images (top) and top-side microscope photograph (bottom)

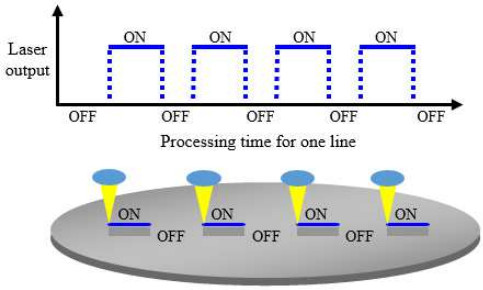


Fig. 8 HASEN cut overview

on and off in a repeated manner, is applied. A schematic illustration of the HASEN cut concept is shown in Fig. 8.

3. Summary

Demand for GaAs substrates is expected to continue to grow for applications such as wireless devices for 5G/6G communications and laser light sources for short-range optical communications. This paper has reported on chipping reduction achieved using specially treated electroformed blades, an ablation process that eliminates wet etching to reduce environmental impact, and application examples of stealth dicing as a dry process. These dicing technologies are expected to broaden the range of options available in device design and manufacturing, while also contributing to improved reliability of electronic and optoelectronic devices based on GaAs substrates.

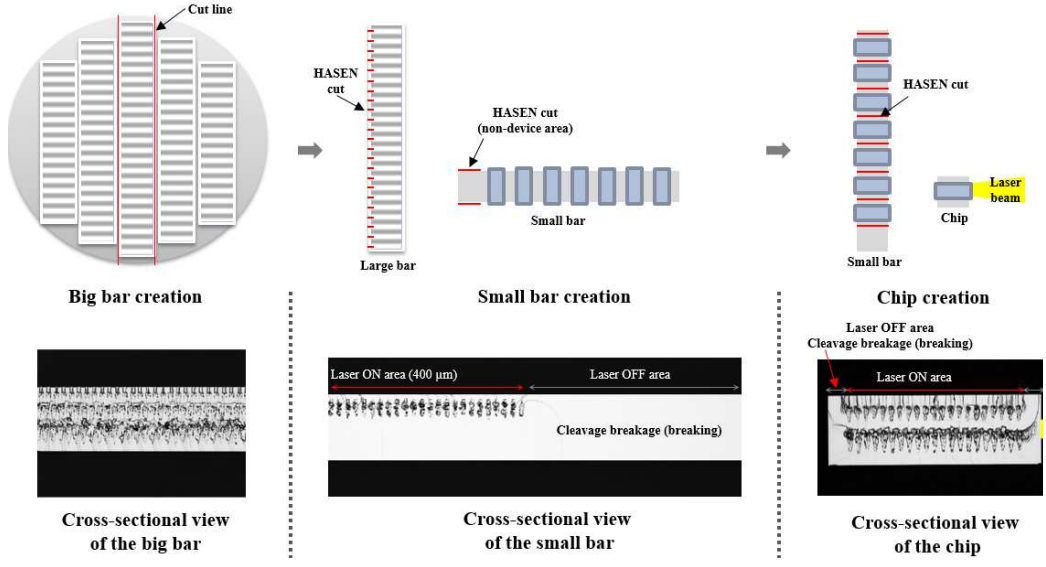


Fig. 7 Edge-emitting diode processing method using stealth dicing